A 10b 1MS/s 0.5mW SAR ADC with double sampling technique

Lee T., Kim M.-Y., Kim Y., Pham P.-H.

Dept. of Electrical Engineering, Korea University, Seoul, South Korea; Department of Electrical Engineering, Texas A and M University, TX, United States; Faculty of Electronics and Telecommunication, Vietnam National University, Hanoi, Viet Nam

Abstract: This paper introduces the 10b 1MS/s 0.5mW SAR ADC with double sampling technique. It utilizes the double sampling technique to reduce power. The SAR ADC is implemented in CMOS 1P8M 65nm technology and occupies 0.111um ^{2}. The maximum sampling rate is 1MS/s. The simulated SNDR and SFDR are 55.6dB and 62.7dB, respectively at input frequency of 484kHz. Power consumption of the data converter is total 507uW with 1.2-V supply. ??2009 IEEE.

Author Keywords: 1MS/s, 10b, 1mW; ADC; Data converter; Double sampling; SAR

Index Keywords: 65nm technology; Data converter; Double sampling; Double sampling technique; Input frequency; Power Consumption; Sampling rates; SAR ADC; Programmable logic controllers; Multicarrier modulation

Year: 2009

Source title: 2009 International SoC Design Conference, ISOCC 2009

Art. No.: 5423831

Page : 512-515

Link: Scorpus Link

Correspondence Address: Lee, T.; Dept. of Electrical Engineering, Korea University, Seoul, South Korea

Conference name: 2009 International SoC Design Conference, ISOCC 2009

Conference date: 22 November 2009 through 24 November 2009

Conference location: Busan

Conference code: 80004

ISBN: 9.78E+12

DOI: 10.1109/SOCDC.2009.5423831

Language of Original Document: English

Abbreviated Source Title: 2009 International SoC Design Conference, ISOCC 2009

Document Type: Conference Paper

Source: Scopus

Authors with affiliations:

1. Lee, T., Dept. of Electrical Engineering, Korea University, Seoul, South Korea
2. Kim, M.-Y., Dept. of Electrical Engineering, Korea University, Seoul, South Korea
3. Kim, Y., Department of Electrical Engineering, Texas A and M University, TX, United States
4. Pham, P.-H., Faculty of Electronics and Telecommunication, Vietnam National University, Hanoi, Viet Nam

References:

1. Lin, Y.M., Kim, B., Gray, P.P., A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3um CMOS (1991) IEEE J. Solid-state Circuits, 26, pp. 628-635. , Apr
2. Scott, M.D., Boser, B.E., Pister, K.S.J., An Ultra-Energy ADC for Smart Dust (2003) IEEE J. Solid-state Circuits, 38, pp. 1123-1129. , Jul
3. Poulton, K., Neff, R., Muto, A., Liu, W., Burstein, A., Heshami, M., A 4GSamples/s 8b ADC in 0.35um CMOS (2002) ISSCC Digest of Technical Papers, , Feb
4. Chen, S.M., Brodersen, R.W., A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS (2006) IEEE J. Solid-state Circuits, 41, pp. 2669-2680. , Dec
5. Taft, R., A 1.8-V 1.6-Gsamples/s 8-b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency (2004) IEEE ISSCC Dig. Tech. Papers, 1, pp. 252-256. , Feb
6. Bult, K., Buchwald, A., An embedded 240-mW 10-b 50 MS/s CMOS ADC in 1-mm2 (1997) IEEE J. Solid-State Circuits, 32 (12), pp. 1887-1895. , Dec
7. Louwsma, S.M., Van Tuijl, E.J.M., Vertregt, M., Nauta, B., A 1.35 GS/s, 10b, 175 mW Time-Interleaved AD Converter in 0.13 um CMOS Symposium on VLSI Circuits Digest of Tehnical Papers, 2007
8. Singh, P.N., Kumar, A., Debnath, C., Malik, R., 20mW, 125 Msps, 10 bit Pipelined ADC in 65nm Standard Digital CMOS Process (2007) IEEE 2007 Custom Integrated Circuits Conference, pp. 189-192. , Sep
9. Sumanen, L., Waltari, M., Kari, A., Halonen, I., A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter (2001) IEEE J. Solid-State Circuits, 36 (7), pp. 1048-1055. , July