A 10b 1MS/s 0.5mW SAR ADC with double sampling technique

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Abstract: This paper introduces the 10b 1MS/s 0.5mW SAR ADC with double sampling technique. It utilizes the double sampling technique to reduce power. The SAR ADC is implemented in CMOS 1P8M 65nm technology and occupies 0.111um². The maximum sampling rate is 1MS/s. The simulated SNDR and SFDR are 55.6dB and 62.7dB, respectively at input frequency of 484kHz. Power consumption of the data converter is total 507uW with 1.2-V supply. ??2009 IEEE.

Author Keywords: 1MS/s, 10b, 1mW; ADC; Data converter; Double sampling; SAR

Index Keywords: 65nm technology; Data converter; Double sampling; Double sampling technique; Input frequency; Power Consumption; Sampling rates; SAR ADC; Programmable logic controllers; Multicarrier modulation

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