

Advanced Microprocessors and Peripherals

Architecture, Programming and Interfacing

Second Edition

File no.
F86
35000
origie

Contents

Preface to the Second Edition

Preface to the First Edition

Acknowledgements

1. The Processors: 8086/8088— Architectures, Pin Diagrams and Timing Diagrams

- 1.1 Register Organisation of 8086 2
- 1.2 Architecture 3
- 1.3 Signal Descriptions of 8086 8
- 1.4 Physical Memory Organisation 14
- 1.5 General Bus Operation 16
- 1.6 I/O Addressing Capability 17
- 1.7 Special Processor Activities 18
- 1.8 Minimum Mode 8086 System and Timings 21
- 1.9 Maximum Mode 8086 System and Timings 25
- 1.10 The Processor 8088 28
- Summary 36*
- Exercises 36*

2. 8086/8088 Instruction Set and Assembler Directives

- 2.1 Machine Language Instruction Formats 38
- 2.2 Addressing Modes of 8086 41
- 2.3 Instruction Set of 8086/8088 46
- 2.4 Assembler Directives and Operators 74
- Summary 82*
- Exercises 83*

3. The Art of Assembly Language Programming with 8086/8088

- 3.1 A Few Machine Level Programs 85
- 3.2 Machine Coding the Programs 91
- 3.3 Programming with an Assembler 95
- 3.4 Assembly Language Example Programs 103
- Summary 129*
- Exercises 129*

Special Architectural Features and Related Programming	131
4.1 Introduction to Stack	131
4.2 Stack structure of 8086/88	133
4.3 Interrupts and Interrupt Service Routines	138
4.4 Interrupt Cycle of 8086/8088	138
4.5 Non Maskable Interrupt	141
4.6 Maskable Interrupt (INTR)	141
4.7 Interrupt Programming	142
4.8 Passing Parameters to Procedures	145
4.9 Handling Programs of Size More than 64K	148
4.10 MACROS	150
4.11 Timings and Delays	152
<i>Summary</i>	155
<i>Exercises</i>	155
Basic Peripherals and Their Interfacing with 8086/88	157
5.1 Semiconductor Memory Interfacing	158
5.2 Dynamic RAM Interfacing	167
5.3 Interfacing I/O Ports	173
5.4 PIO 8255 [Programmable Input-Output Port]	184
5.5 Modes of Operation of 8255	187
5.6 Interfacing Analog to Digital Data Converters	212
5.7 Interfacing Digital to Analog Converters	224
5.8 Stepper Motor Interfacing	228
5.9 Control of High Power Devices Using 8255	231
<i>Summary</i>	232
<i>Exercises</i>	233
Special Purpose Programmable Peripheral Devices and Their Interfacing	235
6.1 Programmable Interval Timer 8253	235
6.2 Programmable Interrupt Controller 8259A	249
6.3 The Keyboard/Display Controller 8279	266
6.4 Programmable Communication Interface 8251 USART	278
<i>Summary</i>	290
<i>Exercises</i>	290
DMA, Floppy Disk and CRT Controllers	293
7.1 DMA Controller 8257	294
7.2 DMA Transfers and Operations	300
7.3 Programmable DMA Interface 8237	306

131	7.4 Floppy Disk Controller 8272	318
	7.5 CRT Controller 8275	350
	7.6 CRT Controller 6845	368
	<i>Summary</i>	389
	<i>Exercises</i>	389
	 8. Multimicroprocessor Systems	
	8.1 Interconnection Topologies	393
	8.2 Software Aspects of Multimicroprocessor Systems	397
	8.3 Numeric Processor 8087	399
	8.4 I/O Processor 8089	420
	8.5 Bus Arbitration and Control	423
	8.6 Tightly Coupled and Loosely Coupled Systems	428
	8.7 Design of a PC Based Multimicroprocessor System	430
	<i>Summary</i>	442
	<i>Exercises</i>	442
	 9. 80286-80287—A Microprocessor with Memory Management and Protection	
	9.1 Salient Features of 80286	444
	9.2 Internal Architecture of 80286	446
	9.3 Signal Descriptions of 80286	451
	9.4 Real Addressing Mode	454
	9.5 Protected Virtual Address Mode (PVAM)	455
	9.6 Privilege	463
	9.7 Protection	468
	9.8 Special Operations	470
	9.9 80286 Bus Interface	473
	9.10 Basic Bus Operations	474
235	9.11 Fetch Cycles of 80286	475
	9.12 80286 Minimum System Configuration	476
	9.13 Interfacing Memory and I/O Devices with 80286	478
	9.14 Priority of Bus Use by 80286	481
	9.15 Bus Hold and HLDA Sequence	484
	9.16 Interrupt Acknowledge Sequence	485
	9.17 Instruction Set Features	486
	9.18 80287 Math Coprocessor	492
	<i>Summary</i>	503
	<i>Exercises</i>	503
293	 10. 80386-80387 and 80486 the 32-Bit Processors	
	10.1 Salient Features of 80386DX	506
	10.2 Architecture and Signal Descriptions of 80386	506

10.3	Register Organization of 80386	510
10.4	Addressing Modes	512
10.5	Data Types of 80386	514
10.6	Real Address Mode of 80386	514
10.7	Protected Mode of 80386	515
10.8	Segmentation	516
10.9	Paging	518
10.10	Virtual 8086 Mode	520
10.11	Enhanced Instruction Set of 80386	523
10.12	The Coprocessor 80387	524
10.13	The CPU with a Numeric Coprocessor—80486DX	528
	<i>Summary</i>	539
	<i>Exercises</i>	540

I. Recent Advances in Microprocessor Architectures— A Journey from Pentium Onwards

542

11.1	Salient Features of 80586 (Pentium)	543
11.2	A Few Relevant Concepts of Computer Architecture	544
11.3	System Architecture	544
11.4	Branch Prediction	548
11.5	Enhanced Instruction Set of Pentium	548
11.6	What is MMX?	549
11.7	Intel MMX Architecture	549
11.8	MMX Data Types	550
11.9	Wraparound and Saturation Arithmetic	550
11.10	MMX Instruction Set	550
11.11	Salient Points About Multimedia Application Programming	552
11.12	Journey to Pentium-Pro and Pentium-II	552
11.13	Pentium III (P-III)—The CPU of the Next Millennium	554
	<i>Summary</i>	554
	<i>Exercises</i>	555

2. Pentium 4—Processor of the New Millennium

556

12.1	Genesis of Birth of Pentium 4	556
12.2	Salient Features of Pentium 4	557
12.3	Netburst Microarchitecture for Pentium 4	558
12.4	Instruction Translation Lookaside Buffer (ITLB) and Branch Prediction	562
12.5	Why Out of Order Execution	562
12.6	Rapid Execution Module	564
12.7	Memory Subsystem	564
12.8	Hyperthreading Technology	565
12.9	Hyperthreading in Pentium	566

- 12.10 Extended Instruction Set in Advanced Pentium Processors 568
- 12.11 Instruction Set Summary 573
- 12.12 Need for Formal Verification 584
 - Summary* 584
 - Exercises* 584

13. RISC Architecture — An Overview

- 13.1 A Short History of RISC Processors 586
- 13.2 Hybrid Architecture—RISC and CISC Convergence 586
- 13.3 The Advantages of RISC 587
- 13.4 Basic Features of RISC Processors 587
- 13.5 Design Issues of RISC Processors 588
- 13.6 Performance Issues in Pipelined Systems 589
- 13.7 Architecture of Some RISC Processors 591
- 13.8 Architecture of Some RISC Processors 596
 - Summary* 596
 - Exercises* 596

14. Microprocessor Based Aluminium Smelter Control

- 14.1 General Process Description of an Aluminium Smelter 598
- 14.2 Normal Control of Electrolysis Cell 599
- 14.3 Cell Abnormalities in an Aluminium Smelter 600
- 14.4 Brief Description of the Control Laws for Abnormal Cells 601
- 14.5 Salient Issues in Design 602
- 14.6 Smelter Controller Hardware 602
- 14.7 Control Algorithm 603
 - Summary* 607

15. Design of a Microprocessor Based Pattern Scanner System

- 15.1 Organization of the Scanner System 609
- 15.2 Description of the Scanning System 611
- 15.3 Programmed Mode of Operation 613
- 15.4 Memory Read/Write System and Start-up Procedures 615
- 15.5 Result and Discussion 616
 - Summary* 618

16. Design of an Electronic Weighing Bridge

- 16.1 Design Issues 620
- 16.2 Software Development 635
- 16.3 Calibration 645
 - Summary* 646

17. An Introduction to Microcontrollers 8051 and 80196

- 17.1 Intel's Family of 8-bit Microcontrollers 649
- 17.2 Architecture of 8051 649
- 17.3 Signal Descriptions of 8051 652
- 17.4 Register Set of 8051 654
- 17.5 Important Operational Features of 8051 655
- 17.6 Memory and I/O Addressing by 8051 658
- 17.7 Interrupts of 8051 661
- 17.8 Instruction Set of 8051 662
- 17.9 Design of a Microcontroller 8051 Based Length
Measurement System for Continuously Rolling
Cloth or Paper 665
- 17.10 Intel's 16-bit Microcontroller Family MCS-96 668
 - Summary* 678
 - Exercises* 679
 - Appendix A* 681
 - Appendix B* 691
 - Appendix C* 707
 - Index***