

A low-power programmable DLL-based clock generator with wide-range anti-harmonic lock

Kim Y., Pham P.-H., Heo W., Koo J.

Department of Electrical and Computer Engineering, Texas A and M, TX, United States; Faculty of Electronics and Telecommunication, Vietnam National University, Hanoi, Viet Nam; Department of Electronics and Computer Engineering, Korea University, Seoul, South Korea

Abstract: A delay-locked loop (DLL)-based clock generator for dynamic frequency scaling has been developed in a 0.13 μ m CMOS technology. The proposed clock generator can generate a wide-range of the multiplied clock signals ranging from 125MHz to 2GHz. In addition, thanks to the proposed anti-harmonic lock block, the clock generator can change the frequency dynamically in one cycle time of the reference clock. The proposed DLL-based clock generator occupies 0.019mm² and consumes 21mW at 2GHz. The ratio of power consumption to frequency of the proposed clock generator is smaller than those of conventional ones. ??2009 IEEE.

Author Keywords: Anti-harmonic lock; Frequency multiplier

Index Keywords: Clock generator; Clock signal; CMOS technology; Cycle time; Delay-locked loops; Dynamic frequency scaling; Frequency multiplier; Low Power; Power Consumption; Reference clock; CMOS integrated circuits; Frequency multiplying circuits; Harmonic analysis; Programmable logic controllers; Electric clocks

Year: 2009

Source title: 2009 International SoC Design Conference, ISOCC 2009

Art. No.: 5423833

Page : 520-523

Link: Scopus Link

Correspondence Address: Kim, Y.; Department of Electrical and Computer Engineering, Texas A and M, TX, United States; email: fcore4@tamu.edu

Conference name: 2009 International SoC Design Conference, ISOCC 2009

Conference date: 22 November 2009 through 24 November 2009

Conference location: Busan

Conference code: 80004

ISBN: 9.78E+12

DOI: 10.1109/SOCCDC.2009.5423833

Language of Original Document: English

Abbreviated Source Title: 2009 International SoC Design Conference, ISOCC 2009

Document Type: Conference Paper

Source: Scopus

Authors with affiliations:

1. Kim, Y., Department of Electrical and Computer Engineering, Texas A and M, TX, United States

2. Pham, P.-H., Faculty of Electronics and Telecommunication, Vietnam National University, Hanoi, Viet Nam
3. Heo, W., Department of Electronics and Computer Engineering, Korea University, Seoul, South Korea
4. Koo, J., Department of Electronics and Computer Engineering, Korea University, Seoul, South Korea

References:

1. Foley, D., Flynn, M.P., CMOS DLL-based 2-V 3.2-ps jitter 1-GHz clock synthesizer and temperature-compensated tunable oscillator (2001) IEEE J. Solid-State Circuits, 36 (3), pp. 417-423. , Mar
2. Chien, G., Gray, P.R., A 900-MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications (2000) IEEE J. Solid-State Circuits, 35 (12), pp. 1996-1999. , Dec
3. Farjad-Rad, R., Dally, W., Ng, H.-T., Senthinathan, R., Lee, M.-J.E., Rathi, R., Poulton, J., A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips (2002) IEEE J. Solid-State Circuits, 37 (12), pp. 1414-1420. , Nov
4. Chung, K., Koo, J., Kim, S.-W., Kim, C., An anti-harmonic, programmable DLL-based frequency multiplier for dynamic frequency scaling Proc. IEEE Asia Solid-State Circuits Conf., Nov. 2007, pp. 276-279
5. Kim, J.-H., Kwak, Y.-H., Kim, M., Kim, S.-W., Kim, C., A 120-MHz-1.8-GHz CMOS DLL-based clock generator for dynamic frequency scaling (2006) IEEE J. Solid-State Circuits, 41 (9), pp. 2077-2082. , Sep
6. Lin, C.-H., Chiu, C.-T., A 2.24GHz wide range low jitter DLL-based frequency multiplier using PMOS active load for communication applications (2007) Proc. IEEE Int. Symp. Circuits and Systems, pp. 3888-3891
7. Kim, C., Hwang, I.-C., Kang, S.-M., A low-power small-area 7.28-ps-Jitter 1-GHz DLL-based clock generator (2002) IEEE J. Solid-State Circuits, 37 (11), pp. 1414-1420. , Nov
8. Farjad-Rad, R., Nguyen, A., Tran, J., Greer, T., Poulton, J., Dally, W., Edmondson, J., Ng, H.-T., A 33-mW 8-Gb/s CMOS clock multiplier and CDR for highly integrated I/Os (2004) IEEE J. Solid-State Circuits, 39 (9), pp. 1553-1561. , Sep
9. Chung, C.-N., Liu, S.-L., A 40GHz DLL-based clock generator in 90nm CMOS technology (2007) ISSCC, Dig. Tech Papers, pp. 178-595. , Feb
10. Chang, H.-H., Lin, J.-W., Liu, S.-L., A fast locking and low jitter delay-locked loop using DHDL (2003) IEEE J. Solid-State Circuits, 38 (2), pp. 343-346. , Feb
11. Jung, Y.-J., Lee, S.-W., Shim, D., Kim, W., Kim, C., Cho, S.-I., A dual-loop delay-locked loop using multiple voltage-controlled delay lines (2001) IEEE J. Solid-State Circuits, 36 (5), pp. 784-791. , May